# Claims

[c1] What is claimed is:

1.A method for increasing network transmission efficiency by increasing a data updating rate of a memory for increasing efficiency of a network interface circuit transmitting data to a network, the network interface circuit including a memory for storing at least one packet transmitted to the network, the method comprising:

storing a packet data corresponding to a packet in the memory;

transmitting the packet data to other sections of the network interface circuit for processing the packet data; and

storing another packet data corresponding to another packet in the memory.

[c2] 2.The method of claim 1 wherein the packet data is completely processed by the other sections of the network interface circuit before another packet data is temporarily stored in the memory.

[c3] 3.The method of claim 1 wherein when a portion of the packet data is processed by the other sections of the network interface circuit before the memory starts to store at least a portion of another packet data for replac-

ing the portion of the packet data.

[c4] 4.The method of claim 1 wherein the operation of the memory is first-in-first-out.

[c5] 5.The method of claim 1 wherein if the packet data is divided into a first portion and a second portion, when the first portion is transmitted to the network and the second portion is not transmitted to the network, the memory starts to store at least a portion of another packet data.

[c6] 6.The method of claim 5 wherein when the memory starts to store at least a portion of another packet data, the first portion of the packet data is overwritten by another packet data.

[c7] 7.The method of claim 5 wherein the memory sequentially stores another packet data for replacing the first portion of the packet data.

[c8] 8.The method of claim 1 wherein the network interface circuit is electrically connected to the memory and a medium control module of the network for processing a plurality of data stored in the memory and for transmitting the processed data to the network; and if the packet data originally stored in the memory is completely processed by the medium control module, the memory

starts to store another packet for replacing the packet data.

[c9] 9. The method of claim 8 wherein when a portion of the packet data processed by the medium control module is transmitted to the network, the memory starts to store another packet for replacing the portion of the packet transmitted to the network.

[c10] 10. The method of claim 8 wherein the medium control module further includes a buffer, and data of the memory must first be stored in the buffer.

[c11] 11. The method of claim 10 wherein the operation of the buffer is first-in-first-out.

[c12] 12. The method of claim 10 wherein when the packet data originally stored in the memory is completely transmitted to the buffer, whether the packet data transmitted to the buffer is transmitted to the network or not, the memory starts to store another packet for replacing the packet data.

[c13] 13. A network interface circuit for controlling data access of a network, the network interface circuit comprising:
a medium control module for transmitting a packet to the network;
a memory for temporarily storing a packet data corre-

sponding to the packet, the memory including a check circuit; wherein after the memory transmits the packet data to the medium control module, the check circuit enables the memory to generate an interrupt request signal; and

a memory access circuit; wherein after receiving the interrupt request signal, the memory access circuit stores another packet data corresponding to another packet in the memory.

[c14] 14. The network interface circuit of claim 13 wherein after the packet data is completely processed by the other sections of the network interface circuit, the check circuit sends the interrupt request signal.

[c15] 15. The network interface circuit of claim 13 wherein when a portion of the packet is processed by the other sections of the network interface circuit, the check circuit sends the interrupt request signal for inputting a portion of another packet.

[c16] 16. The network interface circuit of claim 13 wherein the medium control module further comprises a buffer; wherein before the medium control module completely transmits the packet data of the memory to the network, the buffer stores the portion of the packet data untransmitted to the network.

[c17] 17. The network interface circuit of claim 13 wherein the operation of the memory is first-in-first-out.

[c18] 18. The network interface circuit of claim 16 wherein the operation of the buffer is first-in-first-out.

[c19] 19. The network interface circuit of claim 13 wherein the network interface circuit is a full duplex network interface circuit.

[c20] 20. The network interface circuit of claim 13 wherein the memory controls all other memory units under a recycling memory unit operation.